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[CIRCUIT AREA MINIMIZATION USING SCALING]

Abstract

A method, system and program product that implements area minimization of a circuit design while respecting the explicit and implicit design constraints, in the form of ground rules and user intent. A longest path algorithm is used to generate a scaling factor. The scaling factor is used to reduce the size of the circuit design to the minimum legal size. The scaling may be followed by application of minpert analysis to correct any errors introduced by the scaling. The resulting design is shrunk (or expanded) with all elements shrinking (or growing) together by the same factor, and with the relative relationships of elements maintained. In addition, the invention is operational in the presence of a positive cycle, can be run with scaling that freezes the sizes of any structure or ground rule, and can be applied to technology migration.